

ZEPHYR AND OPEN AMP

Mohammed Billoo

MAB Labs Embedded Solutions

Zephyr Dev Summit 2024

AGENDA




- Motivation
- OpenAmp in Zephyr
- System Architecture
- Development Process (**WARNING: Yocto ahead!**)
- Common Issues and Resolutions
- Next steps


Mohammed Billoo
(mab@mab-labs.com)



THE SPEAKER



 /mab-embedded

 @mabembedded

- Embedded Software Consultant
- Design Work
 - Medical Devices
 - Scientific Instruments
 - LIDAR
 - Custom ASICs
- Experience/Expertise
 - Zephyr RTOS
 - Embedded Linux
 - GUI-based applications



BIOS FOOD NEWSLETTER

Training/Workshops



www.mab-labs.com



MOTIVATION



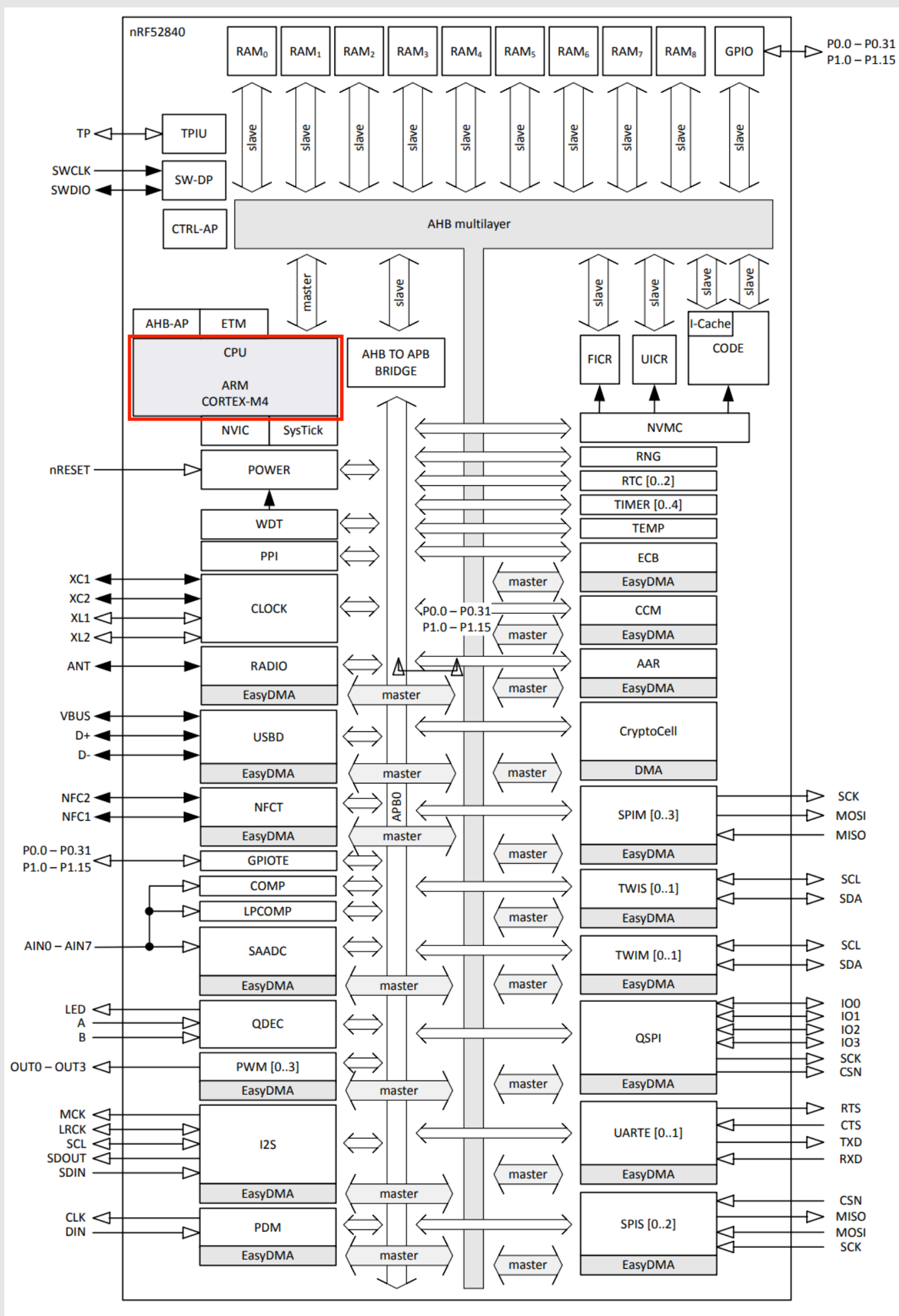
<https://www.electronicproducts.com>

- Heterogenous multi-processor systems
- Traditionally on distinct silicon dice
 - Communication using traditional busses
 - CAN
 - UART
 - SPI
- Each MCU responsible for a safety-critical component
- MPU responsible for non-critical components



MOTIVATION

- Silicon density has exploded
- Single silicon die no longer just a single controller
- Entire **hardware** stacks now present on System-on-Chips (SoC)
 - Radio
 - USB
 - Peripherals
 - Etc
- Actual CPU itself occupies ~3% of silicon



https://infocenter.nordicsemi.com/pdf/nRF52840_PS_v1.0.pdf

MOTIVATION



- Add multiple microcontrollers and microprocessors to single die
- Can distribute the workload
 - MCU responsible for realtime operations
 - MPU responsible for non-realtime operations
- Robotics
 - MCU responsible for actuation
 - MPU responsible for GUI/display, communications, etc..



Security

- Arm® TrustZone®
- DRM Ciphers
- Secure Clock
- eFuse Key Storage
- Random Number
- 32 KB Secure RAM

Main CPU Platform

- 4 x Arm® Cortex®-A53
 - 32 KB I-cache
 - 32 KB D-cache
 - Arm NEON™
 - FPU
- 512 KB L2 Cache (ECC)
- Secondary Cores**
 - Tensilica® HiFi 4 DSP
 - Cortex-M7
- 768 KB On-chip RAM (ECC)

Display

- HDMI 2.0a Tx (eARC) with PHY
- MIPI-DSI (4-lane) with PHY
- 1 x LVDS Tx (4 or 8-lane) with PHY

Audio

- 18 x I²S TDM 32 bit at 768 kHz
- SP/DIF Tx and Rx
- eARC (HDMI)
- ASRC
- 8-ch. PDM Microphone Input

Connectivity and I/O

- 2 x USB 3.0/2.0 OTG with PHY
- 2 x Gbit Ethernet with IEEE® 1588, AVB (One also supports TSN)
- 2 x CAN FD
- 1 x PCIe® Gen 3 – 1-lane L1 Substates
- 4 x UART 5 Mbit/s 5 x I²C, 3 x SPI

External Memory

- x16/x32 LPDDR4/DDR4/DDR3L (Inline ECC)
- 3 x SDIO3.0/MMC5.1
- Dual-ch. QuadSPI (XIP) or 1 x OctalSPI (XIP)
- NAND Controller (BCH62)

System Control

- Smart DMA x3
- XTAL
- PLLs
- Watchdog x 3
- PWM x 4
- Timer x 6
- Secure JTAG
- Temperature Sensor

Machine Learning

- Machine Learning Accelerator: 2.25 TOPS

Graphics

- 3D Graphics: GC7000UL
- 2D Graphics: GC520L

Video

- 1080p60 H.265, H.264, VP9, VP8 decoder
- 1080p60 H.265, H.264 encoder

Vision

- Camera ISP (2 x 187 MP/1 x 375 MP) dewarp
- 2 x MIPI-CSI (4-lane) with PHY

NXP iMX8M Plus

Flex Domain

Real-time MCU
Arm® Cortex®-M7
32kB + 32kB Cache
FPU | MPU | NVIC
512kB TCM with ECC

Main CPU Domain
6x Arm Cortex-A55
32kB I-cache | 32kB D-cache
NEON | 64kB L2 Cache | FPU
512kB L3 Cache (ECC)

Flex Domain
x32 LPDDR5/LPDDR4X (Inline ECC)

System Control
DMA
Watchdog, Periodic Timer
Timer/PWM, Timer
Temperature Sensor

Low Power Real Time Domain
Low Power (Safety) MCU
Arm Cortex-M33
16kB+16kB Cache
FPU | MPU | NVIC
256kB OCRAM (ECC)

Connectivity & I/O
UART/USART/SPI
I²C/I3C/CAN-FD
8-ch PDM Mic Input
Medium Quality Sound Output
2-lane I2S TDM Tx/Rx

EdgeLock® Secure Enclave
Crypto | Tamper Detection | Secure Clock | Secure Boot | eFuse Key Storage | Random Number

System Control
DMA
Watchdog, Periodic Timer
Timer/PWM, Timer
Secure JTAG
V2X Cryptographic Accelerator

Flex Domain
ML & Multimedia
15-lane I²S TDM Tx/Rx, SPDIF
eARC Rx
2x MIPI-CSI 4-lane
1x MIPI-DSI 4-lane
2x 4-lane or 1x 8-lane LVDS
NXP ISP
Arm® Mali™ GPU
VPU + 2D GPU
eIQ® Neutron NPU

Connectivity & I/O
UART/USART/SPI
I²C / I3C
CAN-FD
FlexIO
ADC (8-channel, 12-bit)
2xGbE (TSN) + 10GbE (TSN)
USB 3.0 + USB 2.0
2x PCIe Gen 3.0 x1
XSPI responder

NXP iMX95

MOTIVATION



<https://www.toradex.com/videos/taq-the-balancing-robot>



ADVANTAGES



- Increased speed and reduced latency
 - Massive!
 - On-chip interconnects >> traditional protocols
- OTA simplified
 - MCU firmware resident on MPU filesystem
 - MCU OTA can be part of overall OTA

OPENAMP IN ZEPHYR



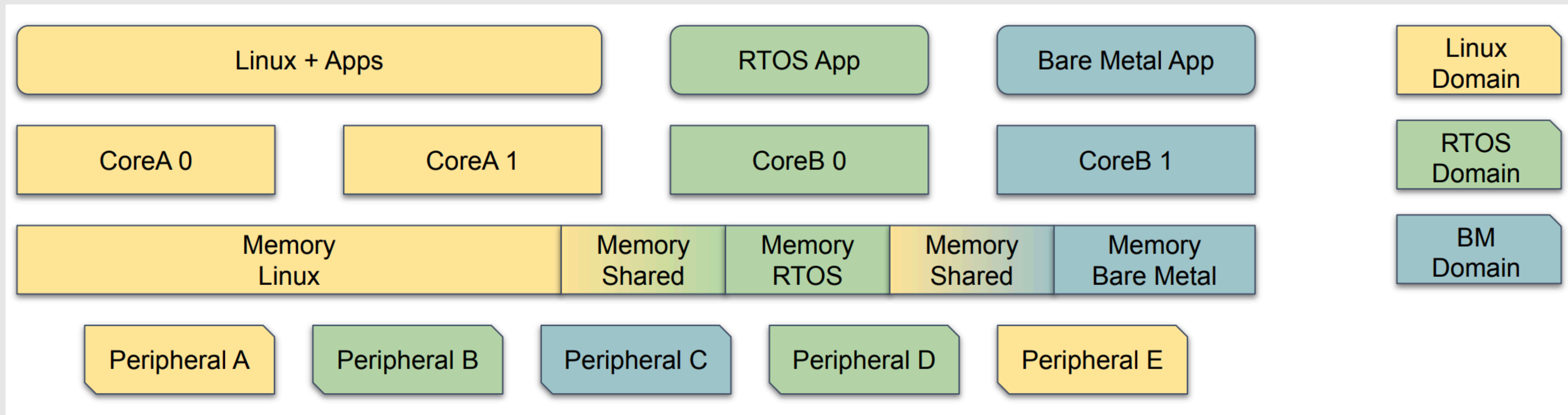
- OpenAMP (<https://github.com/OpenAMP>) **framework**
 - Multiple components
 - OpenAMP library
- Remoteproc and RPMsg
 - Core building blocks of library

OPENAMP IN ZEPHYR



- Remoteproc/RPMsg originally committed to Linux kernel by TI
 - Linux \leftrightarrow SYS/BIOS (i.e. TI/RTOS)
- Picked up by OpenAMP
 - Expanded beyond just Remoteproc/RPMsg into a complete framework
- “OpenAMP Project”
 - openampproject.org

OPENAMP IN ZEPHYR



<https://www.openampproject.org/docs/presentations/OpenAMP-Elevator-Pitch-2024-Q1.pdf>

OPENAMP IN ZEPHYR



- Remoteproc
 - Parses ELF file
 - Ensure that it has appropriate memory segments to be loaded (**important later**)
 - Loads remote processor firmware
 - Starts the remote firmware

OPENAMP IN ZEPHYR



- RPMsg
 - IPC communication mechanism
 - Defines message format
 - RPMsg header
 - Defines source, destination, payload size

OPENAMP IN ZEPHYR



- VirtIO
 - Abstract out IPC
 - Use shared memory region between processors
- Metal
 - Abstraction between OpenAmp and underlying OS
 - Locks, interrupts, DMA, memory, sleep, etc...

OPENAMP IN ZEPHYR



- OpenAmp In Zephyr

```
[zephyrproject]$ ls -l modules/lib/open-amp/open-amp/  
total 172  
drwxrwxr-x 4 mab mab 4096 Jan 9 13:50 cmake  
-rw-rw-r-- 1 mab mab 819 Jan 9 13:50 CMakeLists.txt  
drwxrwxr-x 5 mab mab 4096 Jan 9 13:50 doc  
-rw-rw-r-- 1 mab mab 122997 Jan 9 13:50 Doxyfile  
drwxrwxr-x 8 mab mab 4096 Jan 9 13:50 lib  
-rw-rw-r-- 1 mab mab 4696 Jan 9 13:50 LICENSE.md  
-rw-rw-r-- 1 mab mab 524 Jan 9 13:50 MAINTAINERS.md  
-rw-rw-r-- 1 mab mab 14983 Jan 9 13:50 README.md  
-rw-rw-r-- 1 mab mab 54 Jan 9 13:50 VERSION
```

```
[zephyrproject]$ ls -l zephyr/samples/subsys/ipc/openamp_rsc_table/  
total 24  
drwxrwxr-x 2 mab mab 4096 Jan 9 13:50 boards  
-rw-rw-r-- 1 mab mab 691 Jan 9 13:50 CMakeLists.txt  
-rw-rw-r-- 1 mab mab 248 Jan 9 13:50 prj.conf  
-rw-rw-r-- 1 mab mab 2272 Jan 9 13:50 README.rst  
-rw-rw-r-- 1 mab mab 401 Jan 9 13:50 sample.yaml  
drwxrwxr-x 2 mab mab 4096 Apr 17 12:46 src
```

Zephyr OpenAMP sample using resource table

```
[zephyrproject]$ ls zephyr/lib/open-amp/  
CMakeLists.txt Kconfig resource_table.c resource_table.h
```

OPENAMP IN ZEPHYR



- Relevant Kconfig options

```
CONFIG_IPM=y  
CONFIG_OPENAMP=y  
CONFIG_OPENAMP_RSC_TABLE_NUM_RPMSG_BUFF=8  
CONFIG_OPENAMP_RSC_TABLE=y  
CONFIG_OPENAMP_MASTER=n
```



- Devicetree configuration

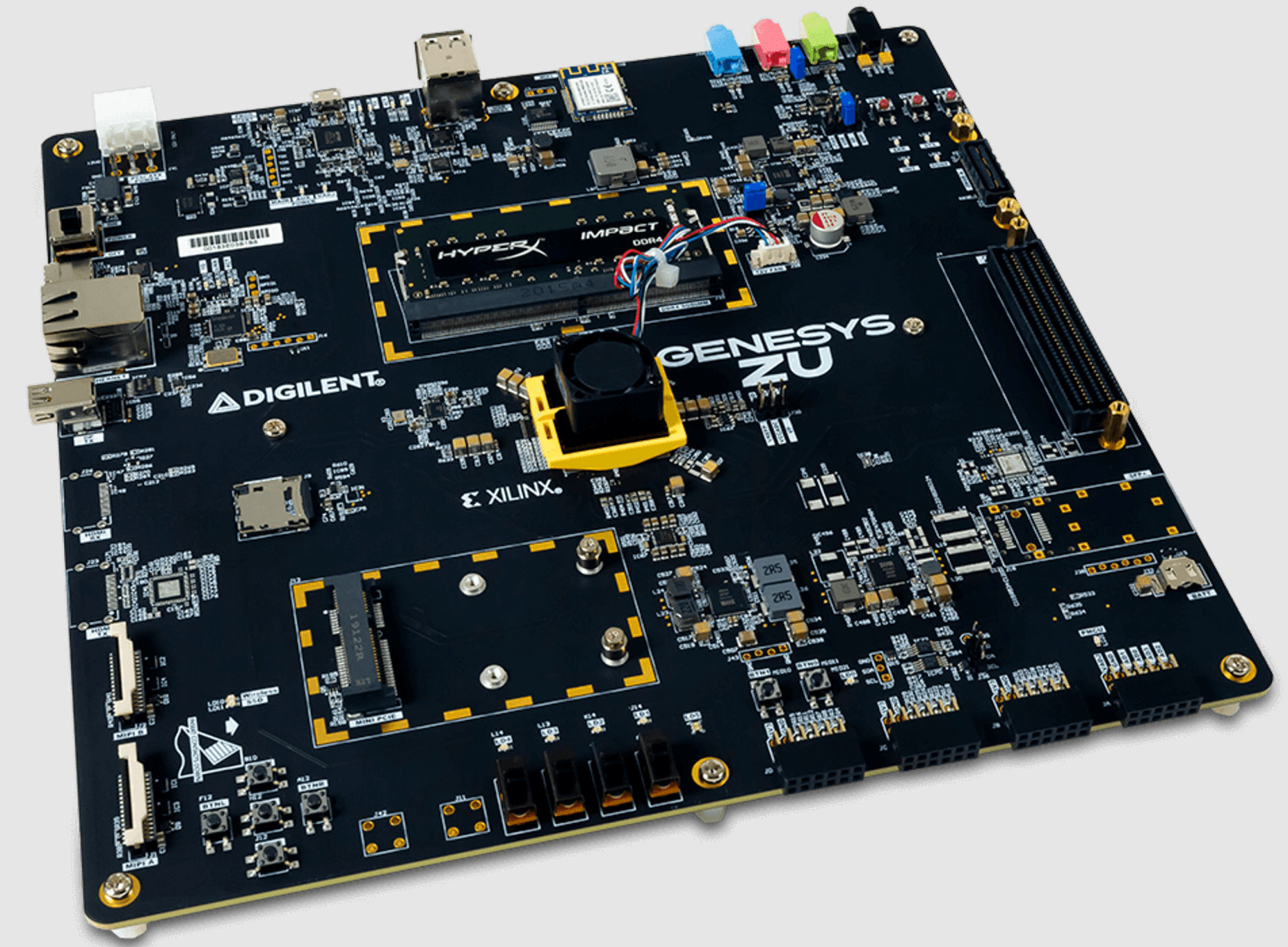
```
1 /*
2  * Copyright (c) 2020, STMICROELECTRONICS
3  *
4  * SPDX-License-Identifier: Apache-2.0
5  */
6
7 / {
8     chosen {
9         /*
10          * shared memory reserved for the inter-processor communication
11          */
12         zephyr,ipc_shm = &mcusram3;
13         zephyr,ipc = &mailbox;
14     };
15
16     mcusram3: memory1@10040000 {
17         compatible = "mmio-sram";
18         reg = <0x10040000 DT_SIZE_K(64)>;
19     };
20 };
21
22 &mcusram {
23     reg = <0x10000000 DT_SIZE_K(256)>;
24 };
```

STM32MP157C_DK2

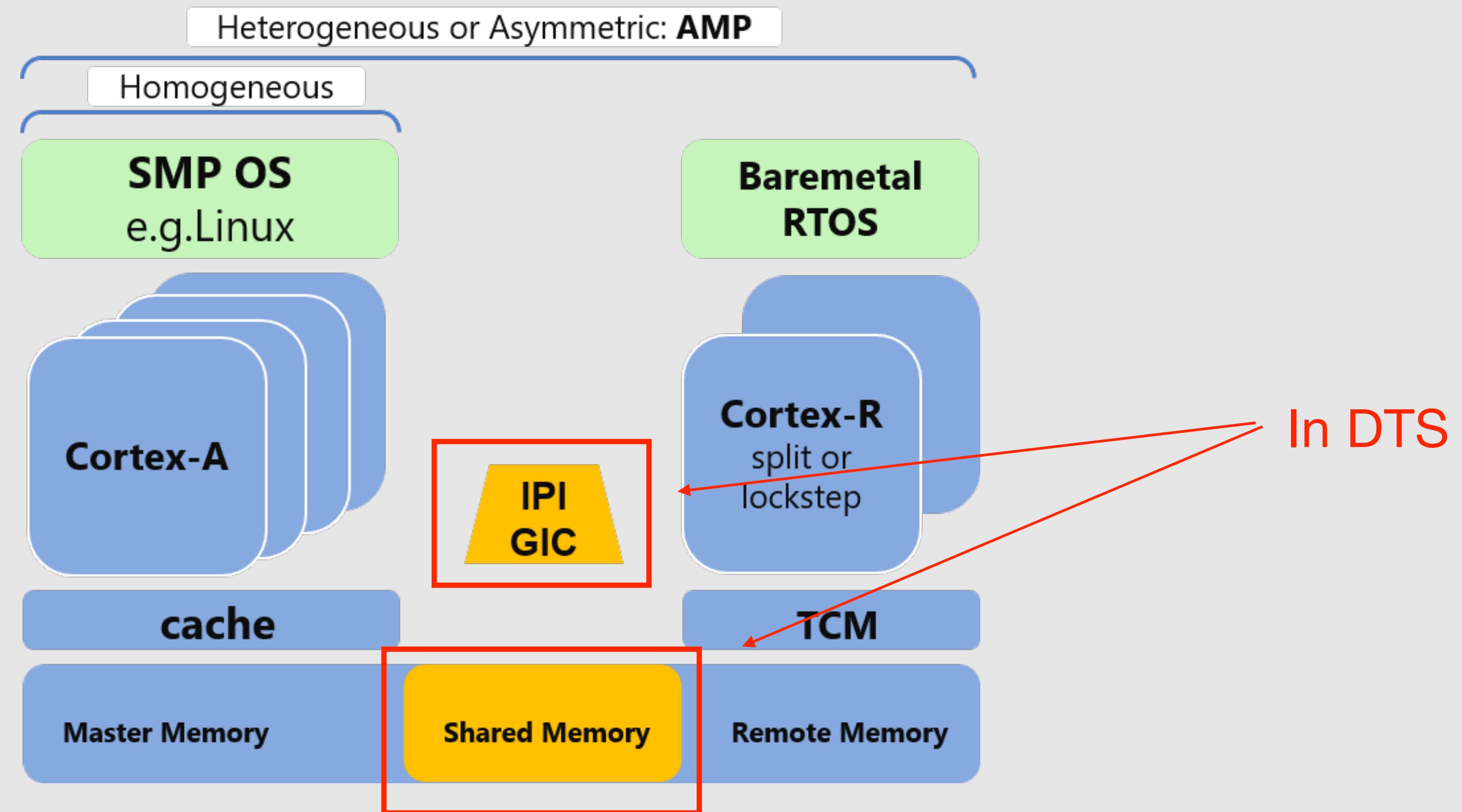
SYSTEM ARCHITECTURE



- Digilent Genesys ZU
 - Zynq MPSoC
 - Quad-core ARM Cortex A53
 - Dual-core ARM Cortex R5

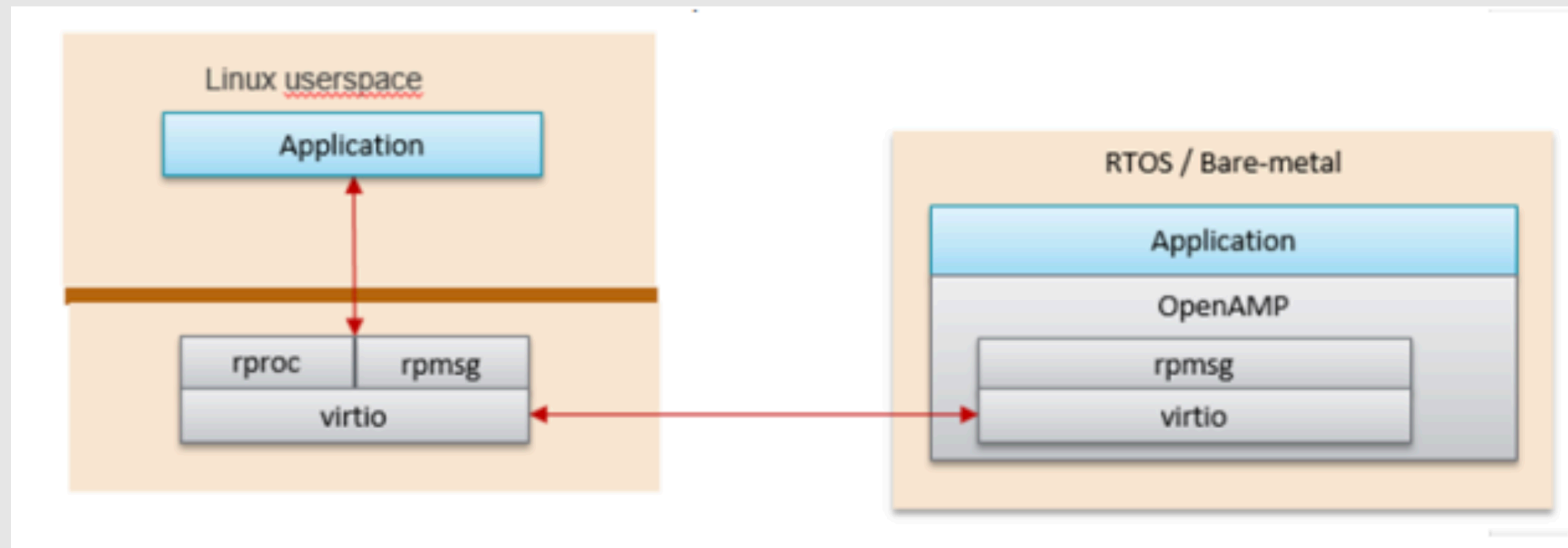


SYSTEM ARCHITECTURE



<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18841718/OpenAMP>

SYSTEM ARCHITECTURE



SYSTEM ARCHITECTURE



- Goal
 - Zephyr firmware for R5 on A53 root filesystem
 - Load Zephyr firmware from (Peta) Linux
 - “Start” Zephyr firmware from Linux
 - Send message from Linux to Zephyr
 - Echo back to Linux

DEVELOPMENT PROCESS



- Use KV260 R5 board in Zephyr as starting point
- Get blinky working
 - Confirm that clock configuration and pinout modifications are correct
 - Use Xilinx tools (i.e. Vitis) to load firmware
 - Use o-scope to confirm blinky frequency
- Test!

DEVELOPMENT PROCESS



- Add remoteproc drivers in Peta Linux

```
Device Drivers --->

Remoteproc drivers --->

# for R5:

<M> ZynqMP_r5 remoteproc support

# for Zynq A9

<M> Support ZYNQ remoteproc
```

DEVELOPMENT PROCESS



- Create recipe to add Zephyr binary to RFS

```
1 #
2 # This file is the openamp-test recipe.
3 #
4
5 SUMMARY = "Simple openamp-test application"
6 SECTION = "PETALINUX/apps"
7 LICENSE = "MIT"
8 LIC_FILES_CHKSUM = "file://${COMMON_LICENSE_DIR}/MIT;md5=0835ade698e0bcf8506ecda2f7b4f302"
9
10 SRC_URI = "file://zephyr.elf \
11           "
12
13 S = "${WORKDIR}"
14
15 INSANE_SKIP_${PN} = "arch"
16
17 RDEPENDS_${PN} = " \
18                 libmetal \
19                 "
20
21 do_install() {
22     install -d ${D}/lib/firmware
23     install -m 0644 ${S}/zephyr.elf ${D}/lib/firmware/zephyr.elf
24 }
25
26 FILES_${PN} = "/lib/firmware/zephyr.elf"
```

DEVELOPMENT PROCESS



- Use Vitis as a debugger
 - Copy over source files
 - Inform Vitis how to reconcile final binary with source files
 - Many-step process
 - Not focus of this talk (maybe another)
 - **Have step through debugging!**

DEVELOPMENT PROCESS



- After boot, instruct Peta Linux to load Zephyr firmware and start

```
echo zephyr > /sys/class/remoteproc/remoteproc0/firmware
```

```
echo start > /sys/class/remoteproc/remoteproc0/state
```

COMMON ISSUES AND RESOLUTIONS



- Issue when loading and starting firmware
 - **CONFIG_OPENAMP_RSC_TABLE=y**
 - Adds resource table section in final ELF
 - Checked by Linux kernel module

COMMON ISSUES AND RESOLUTIONS



- Segfault when sending commands from Linux to Zephyr
 - Zephyr IPC connected to mailbox in DTS?
 - Zephyr SRAM updated to reflect new value?
 - Zephyr SHM node connected to SRAM?

COMMON ISSUES AND RESOLUTIONS



```
rpu0_ipi: zynqmp-ipi@ff310000 {
    status = "disabled";
    compatible = "xlnx,zynqmp-ipi-mailbox";
    #address-cells = <1>;
    #size-cells = <1>;

    reg = <0xff310000 0x10000>;
    reg-names = "host_ipi_reg";
    interrupts = <GIC_SPI 33 IRQ_TYPE_LEVEL
                IRQ_DEFAULT_PRIORITY>;
    local-ipi-id = <1>;

    rpu0_apu_mailbox: mailbox@ff990200 {
        remote-ipi-id = <0>;
        reg = <0xff990200 0x20>,
            <0xff990220 0x20>,
            <0xff990040 0x20>,
            <0xff990060 0x20>;
        reg-names = "local_request_region",
            "local_response_region",
            "remote_request_region",
            "remote_response_region";
    };
};
```

```
&rpu0_ipi {
    status = "okay";
};
```

```
zephyr,ipc = &rpu0_apu_mailbox;
```

COMMON ISSUES AND RESOLUTIONS



```
1 #ifndef SHARED_MEM_PA
2 #if XPAR_CPU_ID == 0
3 #define SHARED_MEM_PA 0x3ED40000UL
4 #else
5 #define SHARED_MEM_PA 0x3EF40000UL
6 #endif /* XPAR_CPU_ID */
7 #endif /* !SHARED_MEM_PA */
8
9 #ifndef SHARED_MEM_SIZE
10 #define SHARED_MEM_SIZE 0x100000UL
11 #endif /* !SHARED_MEM_SIZE */
12
13 #ifndef SHARED_BUF_OFFSET
14 #define SHARED_BUF_OFFSET 0x8000UL
15 #endif /* !SHARED_BUF_OFFSET */
```

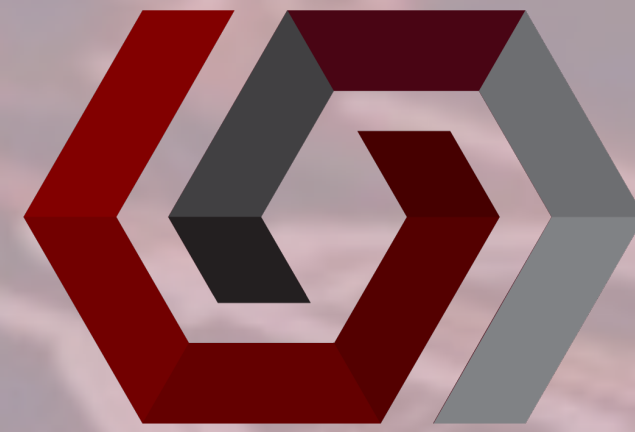
```
&sram0 {
    reg = <0x3ed40000 0x100000>;
};
```

```
zephyr,ipc_shm = &sram0;
```


NEXT STEPS



- Upstream!
 - Add Digilent board to Zephyr
 - Add necessary board overlay to IPC sample
- Document steps to debug Zephyr in Vitis



THANK YOU!

Mohammed Billoo

MAB Labs Embedded Solutions

Zephyr Dev Summit 2024